

1 What is claimed is:

2 1. A method for making a semiconductor device comprising:
3 forming a conductive path on a substrate, the conductive path made of a first
4 material;
5 depositing a second material on the conductive path; and
6 facilitating diffusion of the second material into the conductive path, the second
7 material having a predetermined solubility to substantially diffuse to at least one of an
8 interface and grain boundaries within the first material to significantly increase reliability
9 of the conductive path.

1 2. The method of claim 1, wherein the first material comprises a metal.

1 3. The method of claim 2, wherein the metal is copper.

1 4. The method of claim 3, wherein forming the conductive path comprises a
2 damascene process.

1 5. The method of claim 1, wherein depositing the second material comprises plating
2 the second material on the conductive path.

1 6. The method of claim 5, wherein plating the second material comprises at least
2 one of electroplating, electroless plating, and immersion plating the second material on
3 the conductive path.

1 7. The method of claim 1 further comprising forming a barrier layer between the
2 substrate and the conductive path.

1 8. The method of claim 1, wherein the substrate comprises an interlayer dielectric
2 (ILD).

1 9. The method of claim 1, wherein the second material comprises a noble metal.

1 10. The method of claim 9, wherein the second material further comprises at least
2 one of silver, gold, palladium, ruthenium, rhodium, osmium, iridium, and platinum.

1 11. The method of claim 1, wherein depositing the second material comprises
2 depositing the second material subsequent to a planarization process of the substrate
3 having the conductive path.

1 12. The method of claim 11, wherein depositing the second material comprises
2 removing an oxide from the conductive path, and immersing the conductive path in an
3 aqueous solution having at least the second material.

1 13. The method of claim 1, wherein depositing the second material comprises
2 depositing the second material before a planarization process of the substrate having
3 the conductive path.

1 14. The method of claim 13, wherein depositing the second material comprises
2 removing an oxide from the conductive path, immersing the conductive path in an
3 aqueous solution having at least the second material, and providing a planarization
4 process of the substrate having the conductive path.

1 15. The method of claim 1, wherein facilitating diffusion of the second material
2 comprises heat treating the conductive path having the deposited second material.

1 16. The method of claim 15, wherein heat treating the conductive path comprises
2 annealing the conductive path at a predetermined temperature and time to substantially
3 diffuse the second material to the grain boundaries within the first material, the
4 predetermined temperature and time based at least in part on the first and second
5 material.

1 17. The method of claim 1, wherein the conductive path comprises at least one of a
2 conductive line and a conductive interconnect.

1 18. A semiconductor device comprising:
2 a conductive path formed on a substrate, the conductive path made of a first
3 material; and
4 a second material deposited on the conductive path, the second material having
5 a predetermined solubility to substantially diffuse to grain boundaries within the first
6 material to significantly increase reliability of the conductive path.

- 1 19. The semiconductor device of claim 18, wherein the first material comprises a
2 metal.
- 1 20. The semiconductor device of claim 19, wherein the metal is copper.
- 1 21. The semiconductor device of claim 20, wherein the conductive path comprises a
2 conductive path formed by a damascene process.
- 1 22. The semiconductor device of claim 18 further comprising a barrier layer between
2 the substrate and the conductive path.
- 1 23. The semiconductor device of claim 18, wherein the substrate comprises an
2 interlayer dielectric layer (ILD).
- 1 24. The semiconductor device of claim 18, wherein the second material comprises a
2 noble metal.
- 1 25. The semiconductor device of claim 24, wherein the second material further
2 comprises at least one of silver, gold, palladium, ruthenium, rhodium, osmium, iridium,
3 and platinum.
- 1 26. The semiconductor device of claim 18, wherein the conductive path comprises at
2 least one of a conductive line and a conductive interconnect.